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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,516	01/18/2000	Sameer Halepete	TRANS34	9779

7590 07/18/2002

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EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/484,516	Applicant(s) HALEPETE ET AL.	
	Examiner Paul R. Myers	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/7/02 have been fully considered but they are not persuasive.

In regards to applicants argument that the clock generator state machine and voltage regulator are integrated on a single chip. MPEP 2144.04 V B states to make integral is not a patentable distinction. See previous response to applicants repeated arguments.

In regards to applicants argument that the applicants have realized that integrating all these components on a single chip eliminates the various interfaces which slow operation, and allows direct control of the frequency by the processor itself. First these features are not claimed. Second even if they were this is a well known advantage of integrating all components on a single chip. Additional advantages include impedance matching between components without having to compensate with the aluminum/copper to silicone interface and size reduction. Thirdly applicants statement is a mere allegation of unobviousness without a declaration from an expert.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-3, 6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN 5,812,860 in view of Weiss et al PN 5,774,703.

In regards to claim 1: Horden et al teaches a method for controlling the operating condition of a computer processor comprising the steps of: determining a maximum allowable power consumption level from the operating condition of the processor (Column 6 lines 23-25); determining the maximum frequency which provides power not greater than the allowable power consumption level (Column 6 lines 26-30); determining a minimum voltage which allows operation at the maximum frequency determined (Column 6 lines 33-35); and dynamically changing the operating condition of the processor by changing the frequency and voltage to the maximum frequency and minimum voltage determined (Column 6 lines 36-40). Horden et al also teaches the Clock generator, State machine, and Voltage regulator being on a single chip. Horden et al does not expressly teach them being on the same chip as the processor. MPEP 1244.04 V B states making integral is not a patentably distinct. Horden et al does not teach the clock generator being able to provide a plurality of frequencies that can be individually selected concurrently. Weiss et al teaches a clock generator for a processor that provides a plurality of clock frequencies which can be individually selected concurrently. It would have been obvious to provide multiple concurrent frequencies because this would have made it easier to optimize different subsystems of the processor (See Weiss abstract). The examiner notes Weiss et al also has the bonus of teaching the clock generator being integrated on the same chip as the rest of the processor (See column 2 where it states figure 1 is a single chip processor).

In regards to claims 2, 6 and 8: Horden et al teaches a power supply furnishing selectable output voltages (7 and 5); a clock frequency source (8 and 6); a central processor (Figure 1) including: a processing unit (1, 4) for providing values (15) indicative of operating conditions of the central processor; and a clock frequency generator (6) receiving a clock frequency (14) from a clock frequency source (8) and providing a selectable output clock frequency (11) to the processing unit (1, 4); and means for detecting the value indicative of operating conditions of the central processor (6 via 5 and 4) and causing the power supply (7, 5 via 12) and clock frequency generator (6) to furnish an output clock frequency (11) and voltage level (9) for the central processor.

In regards to claims 3 and 9: Horden et al teaches the means for detecting the values including software (4) for determining the output frequency and power.

In regards to claims 10-11: Horden et al teaches adjusting the operating condition of the processor core for optimum operation. Horden et al does not expressly teach the core including a plurality of functional units. Official notice is taken that processor cores with a plurality of functional units is very well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a plurality of functional units in the core because this would have allowed for greater processing capabilities.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

PN 5,914,996 to Huang also teaches a single chip processor that includes multiple internal frequencies.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on 703 305 3477. The fax phone numbers for the organization where this application or proceeding is assigned are 703 746 7239 for regular communications and 703 746 7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 3900.

Paul R. Myers

PRM
July 15, 2002

PAUL R. MYERS
PRIMARY EXAMINER